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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/621,870

07/17/2003

Yong-Soo Kim

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EXAMINER

KENNEDY, JENNIFER M

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/621,870

Applicant(s)

KIM, YONG-SOO

Examiner

Jennifer M. Kennedy

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 January 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 10, 2005 has been entered.

Response to Amendment

In view of Applicant's amendment to the claim, the objections of claim are withdrawn.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the upper electrode of multi-layers of a polysilicon layer and a metal layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3, 10, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haukka et al. (U.S. Patent Appl. 2003/0049942) in view of Lee (U.S. Patent No. 6,355,519, herein after referred to as Lee '519) and Lee (U.S. Patent No. 6,207,528, herein after referred to as Lee '528).

In re claim 1, Haukka et al. disclose the method including:

forming a lower electrode constituted with a silicon layer on a semiconductor substrate by a predetermined process on which a predetermined process has been completed (see paragraph [0068] and Figure 1, wherein the examiner considered the predetermined process that has been completed the cleaning of the substrate);

forming a uniform silicon oxide layer (30, see paragraph [0029] and [0040]) on the lower electrode by performing an atomic layer deposition (ALD) process;

forming an aluminum oxide (Al_2O_3) film on the silicon oxide layer (see [0041], [0043], [0048]-[0056] and Table 1) by using an ALD method, wherein the method for forming the uniform silicon oxide layer and the aluminum oxide film reduces incubation time required for the formation of the Al_2O_3 film on the silicon oxide layer and prevents metallic clusters from forming at an interface between the Al_2O_3 film and the silicon oxide layer.

Haukka et al. does not explicitly disclose that the method for forming the uniform silicon oxide layer and the aluminum oxide film reduces incubation time required for the formation of the Al_2O_3 film on the silicon oxide layer and prevents metallic clusters from forming at an interface between the Al_2O_3 film and the silicon oxide layer, however the examiner asserts that this benefit is inherent in the process of Haukka et al. As pointed about above, the specification of the instant application on page 10, lines 22-25, discusses that it is the formation of the uniform silicon oxide layer that allows for these benefits. It is submitted that the process of forming a silicon oxide by ALD would create a uniform silicon oxide layer. Further, the examiner notes that the method of Haukka et

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al. of forming a silicon oxide layer by ALD and then a subsequent Al_2O_3 film by ALD is identical to the method of the instant application, and thus, the result of the formation would be the same (i.e. reduction of the incubation time required for the formation of the Al_2O_3 film and the removal of metallic clusters formed at an interface between the Al_2O_3 film and the silicon oxide layer).

Haukka et al. does not disclose the method wherein the Al_2O_3 film is crystallized by carrying out a heat treatment process. Lee '519 discloses the method of crystallizing a Al_2O_3 film by a heat treatment process (see column 4, line 60 through column 5, line 27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to crystallize the Al_2O_3 film by a heat treatment process because as Lee '519 teaches it improves the dielectric characteristic.

Haukka et al. and Lee '519 disclose the method as claimed and rejected above, including the method of forming the upper electrode layer of a polysilicon layer or a metal layer (Lee '519; column 5, lines 34-36, and column 4, lines 15-20), but do not disclose the method wherein forming an upper electrode includes forming multi-layers of a polysilicon layer and a metal layer.

Lee '528 disclose the method of forming the upper electrode includes forming multi-layers of a polysilicon layer and a metal layer (see column 1, lines 25-32, and column 5, lines 34-38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the upper electrode of multi-layers of a polysilicon layer and a metal layer because as Lee '528 teaches the multi layer upper electrode of metal and polysilicon is conventional (see column 1, lines 25-32) and

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because the multi-layer electrode of TiN and polysilicon has the benefits of the diffusion barrier properties of titanium nitride, while keeping a sufficiently high conductivity of the polysilicon layer.

In re claim 3, Haukka et al. disclose the method wherein the silicon oxide layer is formed by using an in-situ method or an ex-situ method (see paragraph [0067]).

In re claim 10, Haukka et al. disclose the method wherein $\text{Al}(\text{CH}_3)_3$, which is trimethylaluminum (TMA), is used as an aluminum source, and one of H_2O , O_3 , and H_2O_2 is used as a reaction source during the ALD process to form the Al_2O_3 film (see [0041], [0043], [0048]-[0056] and Table 1).

In re claim 14, Lee '519 discloses the method wherein the heat treatment process is carried out at a temperature greater than 600°C and in an N_2 or O_2 ambient.

In re claim 15, Lee '519 discloses the method wherein the heat treatment process is carried out by using a furnace annealing process or a rapid thermal process (RTP)

In re claim 16, Lee '528 discloses the method wherein an upper electrode constituted with a metal layer; a silicon layer or a metal layer/silicon layer is formed on an area of the a dielectric film (see column 1, lines 25-32, and column 5, lines 34-38).

Claims 4-5 and 7-8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Haukka et al. (U.S. Patent Appl. 2003/0049942), Lee '519 (U.S. Patent No. 6,355,519) and Lee '528 (U.S. Patent No. 6,207,528), in view of Klaus et al. (U.S. Patent No. 6,090,442).

In re claims 4 and 5, Haukka et al., Lee '519, and Lee '528, disclose the method as claimed and rejected above, but do not disclose the particulars of the method of forming the silicon oxide, including wherein the silicon source selected from the group of SiCl_4 , DCS, and HCD and a reaction source selected from a group consisting of H_2O , O_3 , and H_2O_2 are used to form the silicon oxide, and wherein pyridine acting as a catalyst is used when the silicon source and the reaction source are supplied during the ALD process.

Klaus et al. disclose the method wherein the silicon source selected from the group of SiCl_4 , DCS, and HCD and a reaction source selected from a group consisting of H_2O , O_3 , and H_2O_2 are used to form the silicon oxide, and wherein pyridine acting as a catalyst is used when the silicon source and the reaction source are supplied during the ALD process (see column 5, lines 5-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon oxide of Haukka et al. by the method of Klaus et al. because as Klaus et al. discloses the method allows for a low temperature deposition process (see column 10, lines 20-25) which will reduce the thermal budget of forming the capacitor.

In re claim 7, Klaus et al. discloses the method wherein the silicon oxide layer is formed at a low temperature less than about 200 °C (see column 5, lines 5-40, and column 10, lines 20-25).

In re claim 8, Haukka et al. discloses the method wherein a thickness of the silicon oxide is less than about 10 angstroms (see paragraph [0029]).

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haukka et al. (U.S. Patent Appl. 2003/0049942) and Lee '519 (U.S. Patent No. 6,355,519) and Lee '528 (U.S. Patent No. 6,207,528), in view of Tera et al. (U.S. Patent Appl. 2001/0031379).

In re claim 4 and 6, Haukka et al., Lee '519, and Lee '528, disclose the method as claimed and rejected above, but do not disclose the particulars of the method of forming the silicon oxide, including wherein the silicon source selected from the group of SiCl₄, DCS, and HCD and a reaction source selected from a group consisting of H₂O, O₃, and H₂O₂ are used to form the silicon oxide and wherein each of a supply time and a purge time for the silicon source and the reaction source is less than 10 seconds respectively.

Tera et al. disclose the method wherein silicon source selected from the group of SiCl₄, DCS, and HCD and a reaction source selected from a group consisting of H₂O, O₃, and H₂O₂ are used to form the silicon oxide and wherein each of a supply time and a purge time for the silicon source and the reaction source is less than 10 seconds respectively (see Figure 12, and [0104]).

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon oxide layer by the method of Tera et al. because as Tera et al. teaches it allows for a uniform thin dielectric layer of silicon oxide with excellent step coverage (see paragraph [0008] and [0044]) which is desirable in capacitor fabrication.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haukka et al. (U.S. Patent Appl. 2003/0049942) and Lee '519 (U.S. Patent No. 6,355,519) and Lee '528 (U.S. Patent No. 6,207,528), in view of Sarigiannis et al. (U.S. Patent Appl. 2004/0033688).

In re claim 11, Haukka et al., Lee '519, and Lee '528 disclose the method as claimed and rejected above, but do not disclose wherein plasma is used as the energy source during the ALD process to form the Al_2O_3 film.

Sarigiannis et al. discloses the method of utilizing plasma in formation of an Al_2O_3 film by ALD (see paragraph [0017] and [0027]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize plasma in the formation of the Al_2O_3 film in the method of Haukka et al. because adding plasma, as known in the art, reduces the temperature at which the reactions will occur, thus allowing for reduction of the thermal budget of the capacitor.

In re claim 12, Haukka et al., Lee '519, Lee '528 and Sarigiannis et al. do not disclose the method wherein the ALD process to form the Al_2O_3 film is carried out at a

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room temperature or at a temperature of about 500 °C. The examiner notes that 400°C is considered to be “about 500°C”, especially in light of the specification (page 10, lines 9-13), in which the Applicant defines about 500°C to be from a range of about 200°C to about 500°C. Furthermore, the examiner notes that Applicant does not teach that a temperature of “about 500°C” solves any stated problem or is for any particular purpose. Therefore, this temperature lacks criticality in the claimed invention. Haukka et al. teaches the same method at a temperature of about 400°C (see paragraph [0048]). Thus, it would have been obvious to one of ordinary skill in the art to perform steps at “about 500°C” since the invention would perform equally well whether at 400°C or “about 500°C” to provide a temperature capable of forming a high-k dielectric by an ALD process without increasing the thickness of the interfacial dielectric layer (see paragraph [0048]), and because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233, MPEP 2144.05 II A.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haukka et al. (U.S. Patent Appl. 2003/0049942), Lee '519 (U.S. Patent No. 6,355,519) and Lee '528 (U.S. Patent No. 6,207,528), in view of Raaijmakers et al. (U.S. Patent Appl. 2001/0024387).

Haukka et al., Lee '519, and Lee '528 disclose the method as claimed and rejected above, but do not disclose the method wherein a thickness of the Al₂O₃ film is

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less than about 100 angstroms. Raaijmakers et al. discloses the method of forming an Al_2O_3 film to a thickness of less than about 100 angstroms (see paragraph [0083]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the film of Haukka et al. to a thickness of less than about 100 angstroms, because, as Raaijmakers et al. teaches 100 angstroms allows for a sufficiently thick metal oxide that avoids leakage during memory cell operation and allows for near perfect step coverage which is desirable in high surface area, high aspect ratio, capacitor fabrication (see paragraph [0083]).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haukka et al. (U.S. Patent Appl. 2003/0049942) and Lee '519 (U.S. Patent No. 6,355,519) and Lee' 528 (U.S. Patent No. 6,207,528) in view of Yamamoto (U.S. Patent No. 6,232,178).

In re claim 17, Haukka et al., Lee '519, and Lee '528 disclose the method as claimed and rejected above, including that the method of forming the dielectric layer of silicon oxide and aluminum oxide can formed over a silicon bottom electrode for a capacitor (Haukka [0068], but does not expressly disclose that the bottom electrode includes one of an undoped polysilicon layer and doped amorphous silicon layer.

Yamamoto discloses the method of forming the bottom electrode including one of an undoped polysilicon layer and doped amorphous silicon layer (see column 6, lines 4-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the bottom electrode of one of an undoped polysilicon layer

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and doped amorphous silicon layer because as Yamamoto teaches the method allows for formation of HSG, which increases capacitance.

While Applicant claims an undoped polysilicon layer, the method of Applicant's own disclosure (page 9) is to form an undoped polysilicon layer and then subsequently dope the layer. The examiner notes that for a silicon layer to be conductive, and thus be operative for a capacitor, it must be doped. The examiner suggests amending claim 17 to make it clear that the layer, as deposited, is an undoped polysilicon layer.

Response to Arguments

Applicant's arguments with respect to claims 1 and 3-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nguyen (U.S. Patent No. 6,689,220) discloses that plasma enhanced ALD allows for a reduced temperature requirement (see column 2, lines 32-40). Yoshida (U.S. Patent No. 6,246,085) discloses that doped amorphous silicon is conventional in formation of bottom electrodes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk